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EXAMINER				
MOON, SEOKYUN				
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/601,643

Applicant(s)

HATANO ET AL.

Examiner

SEOKYUN MOON

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 January 2008.
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-8 and 10-12 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1-8 and 10-12 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☒ The drawing(s) filed on 24 June 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/003)
Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____

DETAILED ACTION***Response to Arguments***

1. The Applicant's arguments with respect to the newly amended claim 1 have been considered but are moot in view of the new ground(s) of rejection.

In response to the Applicant's arguments regarding the purposes of having features presented in the claim, the fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985).

In response to the Applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. **Claims 1-8 and 11-12** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kaise (US 6,483,495) in view of Taketomi (US 6,528,397).

As to **claim 1**, Kaise [fig. 1a] teaches an image display device ("*active matrix type liquid crystal display device 100*") having an active matrix substrate ("*base substrate 110*") provided with a pixel region ("*display region 140*") [col. 6 lines 3-10] having a plurality of pixels arranged in a matrix configuration

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[fig. 2a], and a drive circuit region ("*drive circuitry region 150*") disposed outside of the pixel region for supplying drive signals to the plurality of pixels via interconnection lines ("*scanning lines 112*" and "*data signal lines 113*") [fig. 2b] [col. 6 lines 58-61],

wherein the drive circuit region ("*drive circuitry region 150*") [fig. 2a] comprises a plurality of stages of circuit sections ("*shift register circuit 131*", "*buffer circuit 132*", and "*sample holding circuit 133*") successively processing an externally supplied display signal (the signal inputted to the "*shift register circuit 131*") to produce a drive signal (the signal outputted from the "*sample holding circuit 133*") to be supplied to the pixel region ("*display region 140*"), each of the plurality of stages of circuit sections having a different function [col. 7 lines 50-67], and the plurality of stages of circuit sections includes a shift register, a digital-to-analog converter, a buffer circuit, and a sampling circuit [col. 3 lines 33-38].

Kaise does not expressly teach active elements being used or included in each of the shift register, the digital-to-analog converter, the buffer circuit, and the sampling circuit.

However, the Examiner takes Office Notice that it is well known in the art to use/include active elements such as thin film transistors to build or design a shift register, a digital-to-analog converter, a buffer circuit, and a sampling circuit of a driver of an image display device.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use an active element such as a thin film transistor to build or design each of a shift register, a digital-to-analog converter, a buffer circuit, and a sampling circuit, since a thin film transistor is well known for fast response speed and is relatively thin to be used in a small electronic component.

Kaise as modified above does not expressly teach that the active elements in each of the shift register, the digital-to-analog converter, and the buffer circuit use roughly-band-shaped-crystal silicon films having grain boundaries as channels of the active elements, wherein each of the grain boundaries of the roughly-band-shaped-crystal silicon films are continuous in generally one direction and the active

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elements in each of the shift register, the digital-to-analog converter, and the buffer circuit have a direction of movement of carriers therein in a direction of the grain boundaries and the active elements in the sampling circuit use granular polysilicon films having loop-like grain boundaries as channels of the active elements.

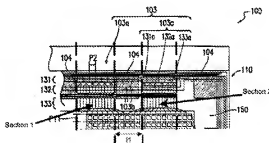
However, Taketomo teaches a concept of forming active elements, i.e. thin film transistors, used in an image display [col. 1 lines 9-11] by using roughly-band-shaped-crystal silicon films ("*polycrystalline silicon thin film 210*") [fig. 12(c) and abstract lines 14-16] having grain boundaries as channels of the active elements [col. 18 lines 7-12], wherein each of the grain boundaries of the roughly-band-shaped-crystal silicon films are continuous in generally one direction [col. 18 lines 7-12 and col. 17 lines 41-43] and the thin film transistors have a direction of movement of carriers therein in a direction of the grain boundaries [col. 18 lines 7-12 and col. 17 lines 41-43] and the thin film transistors use granular polysilicon films having loop-like grain boundaries [fig. 12(c)] as channels of the thin film transistors.

It would have been obvious to one of ordinary skill in the art at the time of the invention to form the active elements of the image display device of Kaise as modified above by using roughly-band-shaped-crystal silicon films having grain boundaries as channels of the active elements, wherein each of the grain boundaries of the roughly-band-shaped-crystal silicon films are continuous in generally one direction and the thin film transistors have a direction of movement of carriers therein in a direction of the grain boundaries and the thin film transistors use granular polysilicon films having loop-like grain boundaries as channels of the thin film transistors, as taught by Taketomo, in order to allow the active elements of the image display device of Kaise as modified above to have high carrier mobility [col. 18 lines 7-12].

As to **claim 2**, Kaise [fig. 2a] teaches that the circuit sections ("*section 1*" and "*section 2*" shown on drawing 1 of this office action, which is equivalent to fig. 2a of Kaise) of each of the plurality of stages ("*shift register circuit 131*", "*buffer circuit 132*", and "*sample holding circuit 133*") are arranged along

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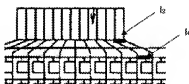
one side (upper side) of the active matrix substrate ("base substrate 110") at specified intervals ("I1" shown on drawing 1) at a periphery thereof.



Drawing 1

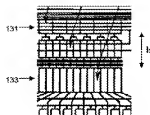
As to **claim 3**, Kaise [fig. 2a] teaches that circuit sections ("sample holding circuit 133") having the active elements formed therein are in a final output stage of the plurality of stages ("shift register circuit 131", "buffer circuit 132", and "sample holding circuit 133") [col. 7 lines 60-62], and

the interconnection lines coupling the final output stage to the plurality of pixels are arranged at wider intervals on a pixel-region side thereof than a final-output- stage side thereof [drawing 2 provided below, which is equivalent to fig. 2a of Kaise: $I_2 < I_4$].



Drawing 2

As to **claim 4**, Kaise [fig. 2A] teaches that the circuit sections ("shift register circuit 131" and "sample holding circuit 133") having the active elements formed therein are arranged in two or more parallel rows along one side of the active matrix substrate at specified intervals ("I5" shown on drawing 3 provided on page 6 of this Office Action, which is equivalent to fig. 2a of Kaise) [col. 2 lines 64-67].



Drawing 3

As to **claim 5**, Kaise [fig. 1b] teaches the active elements (the switching elements included in the "sample holding circuit 133" which is included in "data driver 103") [col. 7 lines 51-54 and lines 60-62] being arranged along two opposed sides of the active matrix substrate ("base substrate 110") at specified intervals at peripheries thereof [drawing 1 provided on page 5 of this Office Action].

As to **claim 6**, Kaise as modified by Taketomi does not expressly disclose that areas of the circuit sections having the active elements formed therein vary with a scale thereof.

However, Examiner takes official notice that it is well known in the art at the time of the invention to increase the size of the circuit sections included in the driving circuitry of a display to provide driving signals for greater number of pixels when the size of the display is increased.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the areas of the circuit section of Kaise as modified by Taketomi to be varied with a scale to accommodate the change on the number of pixels to drive when the size of the display changes.

As to **claim 7**, all of the claim limitations have already been discussed with respect to the rejection of claim 4 except for the circuit sections in one of the two or more rows being offset in longitudinal directions.

Kaise [fig. 2a] teaches that the circuit sections ("sample holding circuit 133") in one of the two or more rows ("shift register circuit 131" and "sample holding circuit 133") are offset in longitudinal directions thereof from the circuit sections in an adjacent one of the two or more rows.

As to **claim 8**, all of the claim limitations have already been discussed with respect to the rejection of claim 7 since the active elements are included in the circuit sections.

As to **claim 11**, Kaise as modified by Taketomi teaches each of the pixels comprising a liquid crystal layer.

Kaise as modified by Taketomi does not teach each of the pixels comprising an organic EL layer.

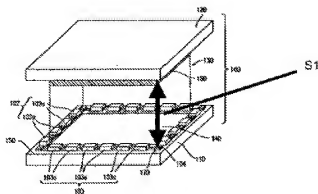
However, since the Applicants have failed to disclose specifying the type of the image display device as an organic EL display, i.e. including an organic EL layer in each of the pixels, provides an advantage, is used for a particular purpose, or solves a state problem, it is an obvious matter of design choice to specify the type of the image display device as an organic EL display.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to specify the type of the image display device in Kaise as modified by Taketomi as any one of a LCD or EL display since any one of the displays having the structure or implementation of the active elements as disclosed would perform equally well at providing superior characteristics in terms of carrier movement.

As to **claim 12**, Kaise as modified by Taketomi teaches the active elements being thin film transistors, as discussed with respect to the rejection of claim 1.

4. **Claim 10** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kaise and Taketomi, as applied to claims 1-8 and 11-12 above, and further in view of Koma (US 6,490,013).

Kaise [fig. 1a] teaches an image display device ("*liquid crystal display device 100*") comprising a liquid crystal layer ("*130*"), wherein the liquid crystal layer is sandwiched between the active matrix substrate ("*base substrate 110*") and a counter substrate ("*120*") superposed on the active matrix substrate with a specified spacing ("*S1*" shown on drawing 4 below, which is equivalent to fig. 1a of Kaise) therebetween.



Drawing 4

Kaise as modified by Taketomi does not expressly disclose having a color filter substrate.

However, Koma teaches a liquid crystal display device having a color filter ("*color filter 38*") [fig. 2] being formed on a counter substrate ("*opposing substrate 30*") [col. 5 lines 8-10].

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement a color filter on the counter substrate of the image display device of Kaise as modified by Taketomi, as taught by Koma, in order to produce adequate colors for each of the plural pixels and thus to provide adequate colors for the images to be displayed on the display device.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

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the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to SEOKYUN MOON whose telephone number is (571)272-5552. The examiner can normally be reached on Mon - Fri (8:30 a.m. - 5:00 p.m.).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

April 21, 2008

/S. M./

Examiner, Art Unit 2629

/Sumati Lefkowitz/

Supervisory Patent Examiner, Art Unit 2629